

FIG. 1

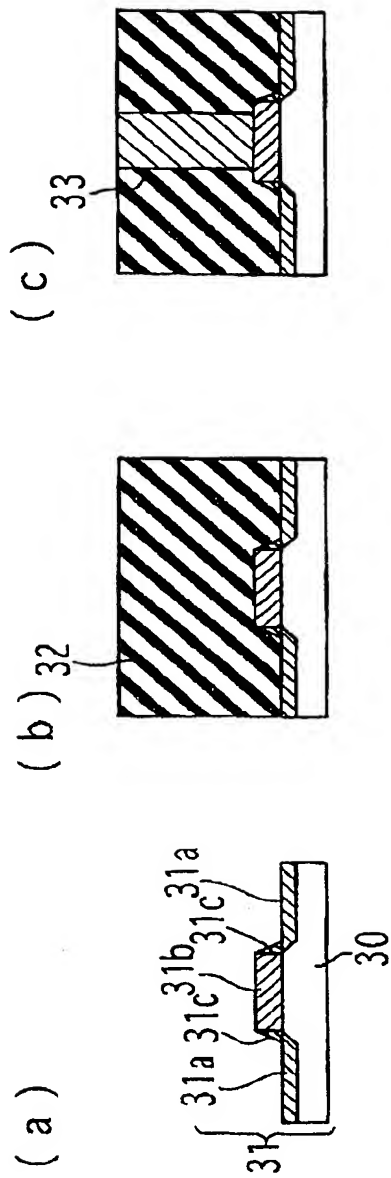


FIG.1

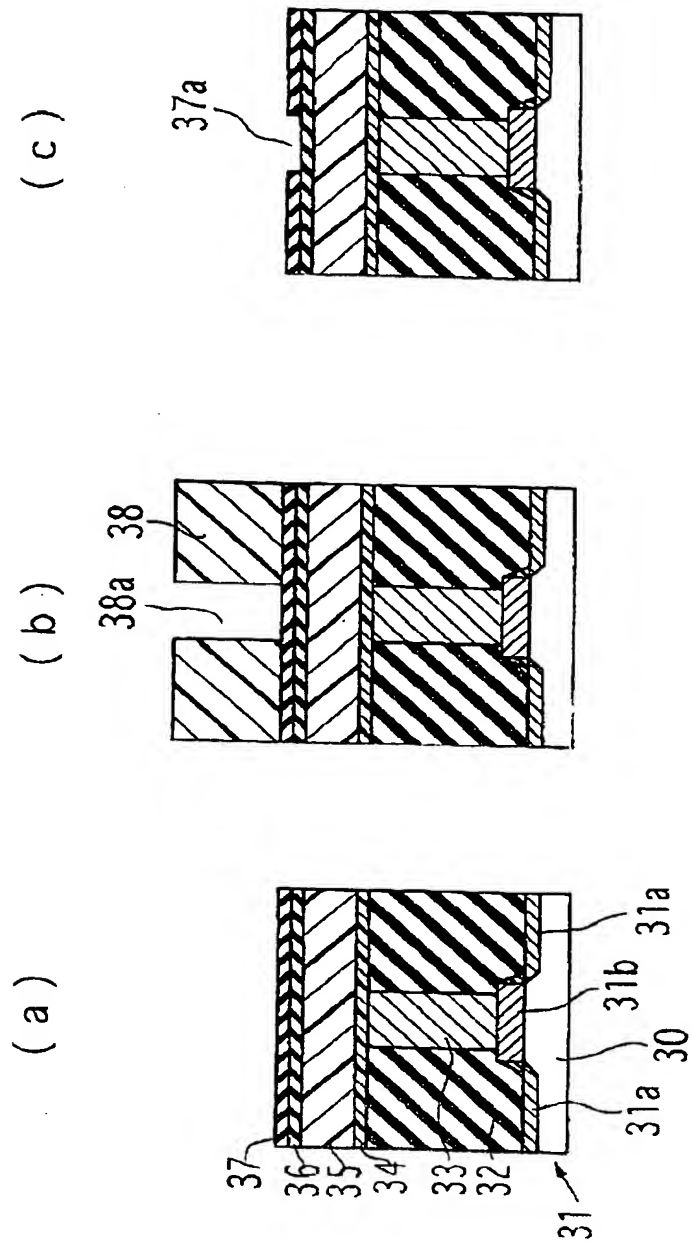


FIG. 2

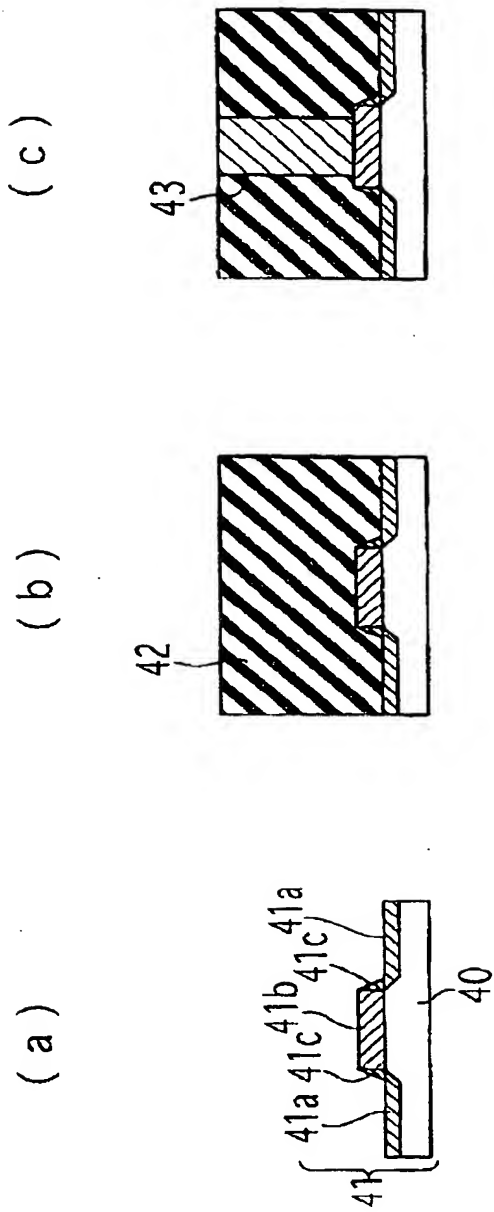


FIG.4

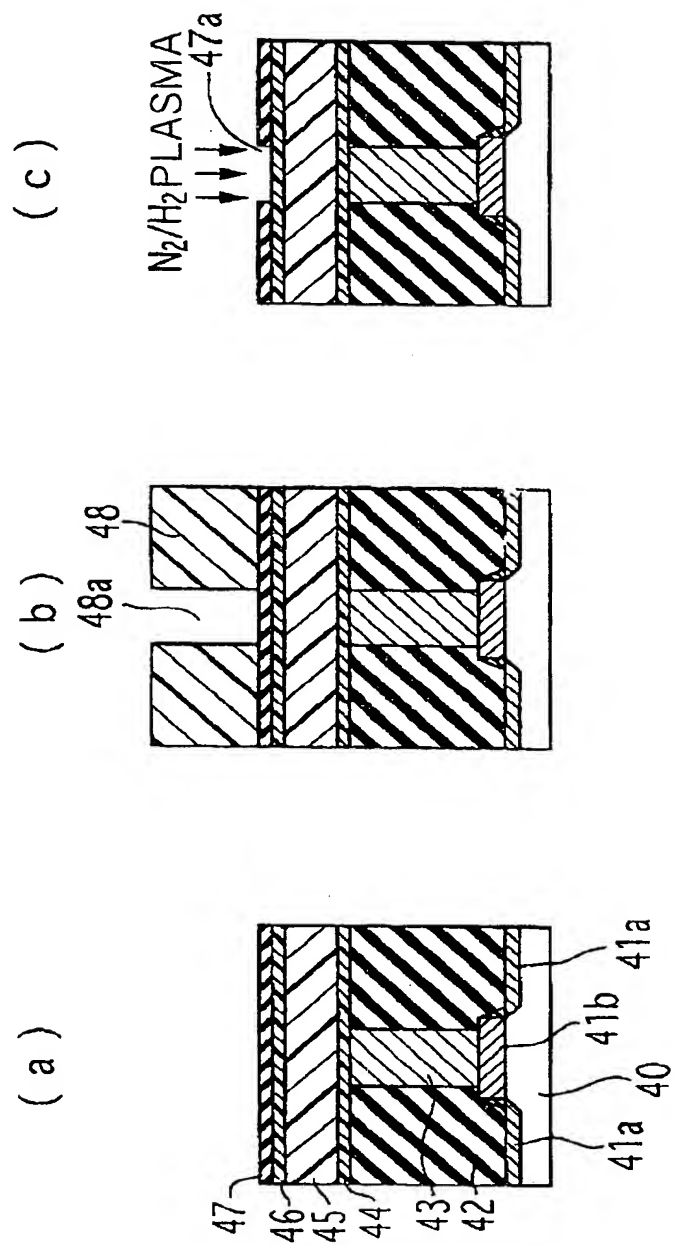


FIG.5

Year	1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100
1970	1971	1972	1973	1974	1975	1976	1977	1978	1979	1980	1981	1982	1983	1984	1985	1986	1987	1988	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000	2001	2002	2003	2004	2005	2006	2007	2008	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019	2020	2021	2022	2023	2024	2025	2026	2027	2028	2029	2030	2031	2032	2033	2034	2035	2036	2037	2038	2039	2040	2041	2042	2043	2044	2045	2046	2047	2048	2049	2050	2051	2052	2053	2054	2055	2056	2057	2058	2059	2060	2061	2062	2063	2064	2065	2066	2067	2068	2069	2070	2071	2072	2073	2074	2075	2076	2077	2078	2079	2080	2081	2082	2083	2084	2085	2086	2087	2088	2089	2090	2091	2092	2093	2094	2095	2096	2097	2098	2099	2100	

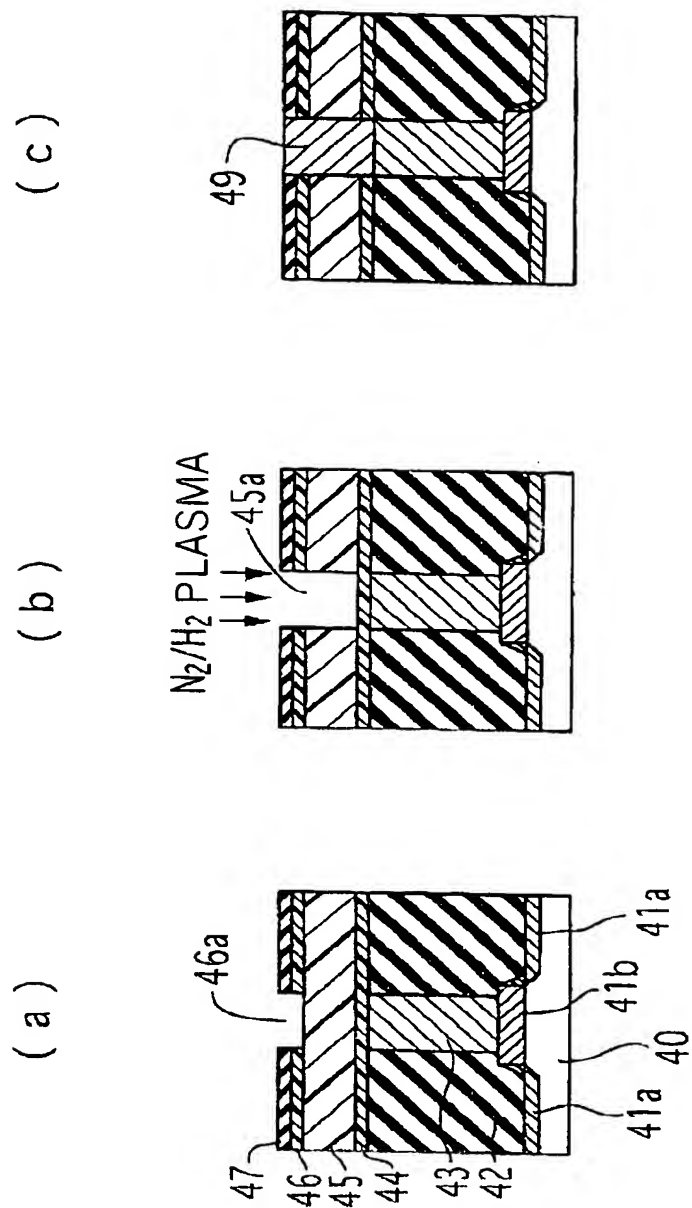


FIG. 6

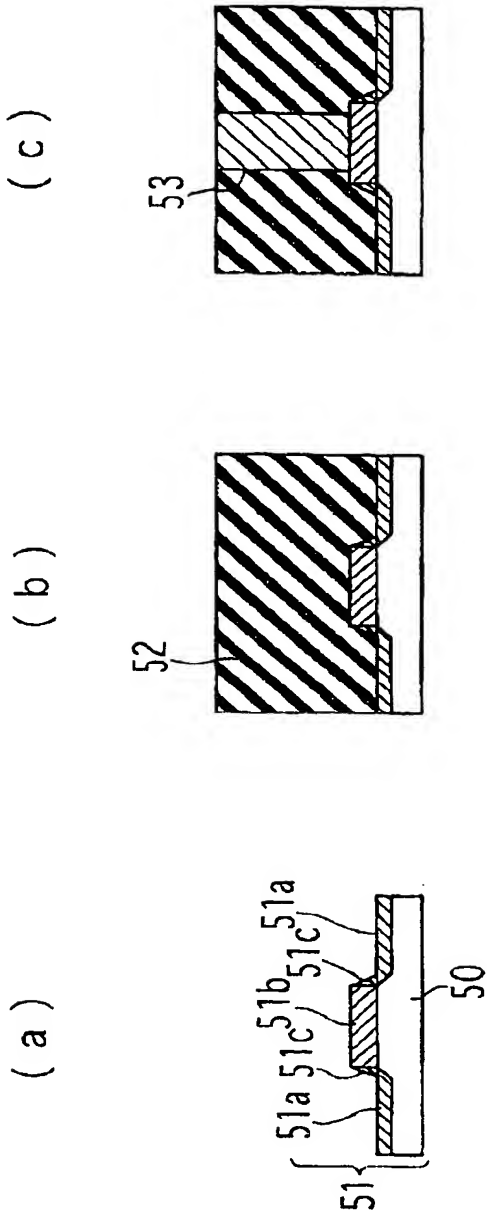


FIG.7

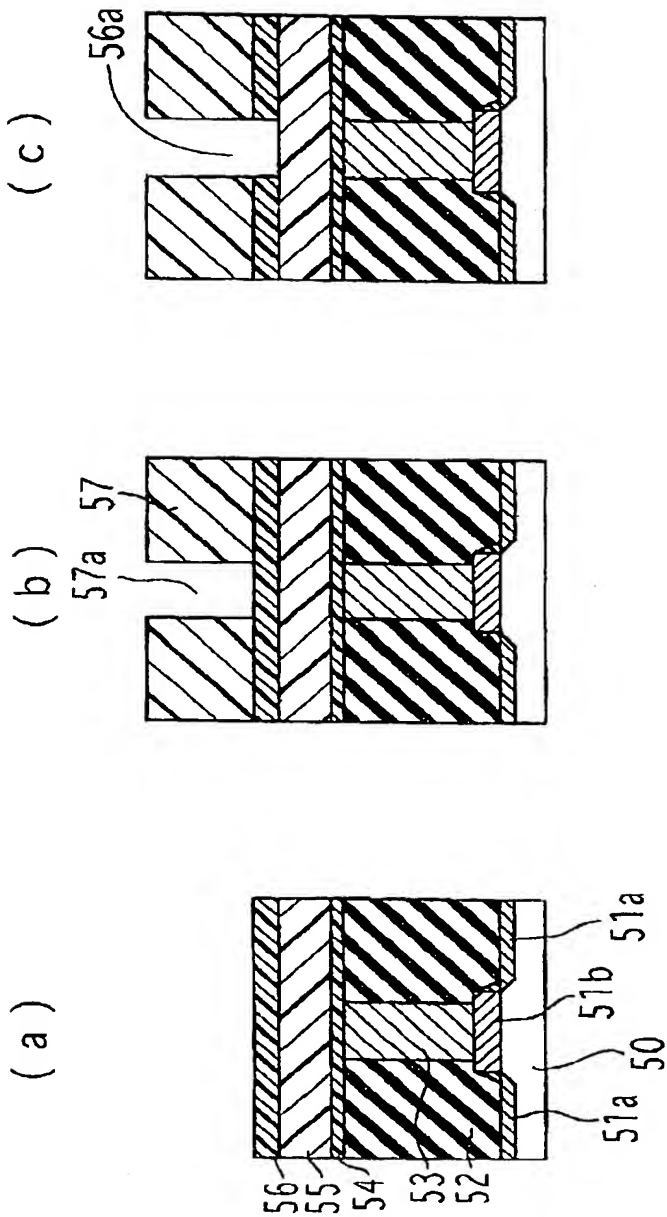


FIG.8

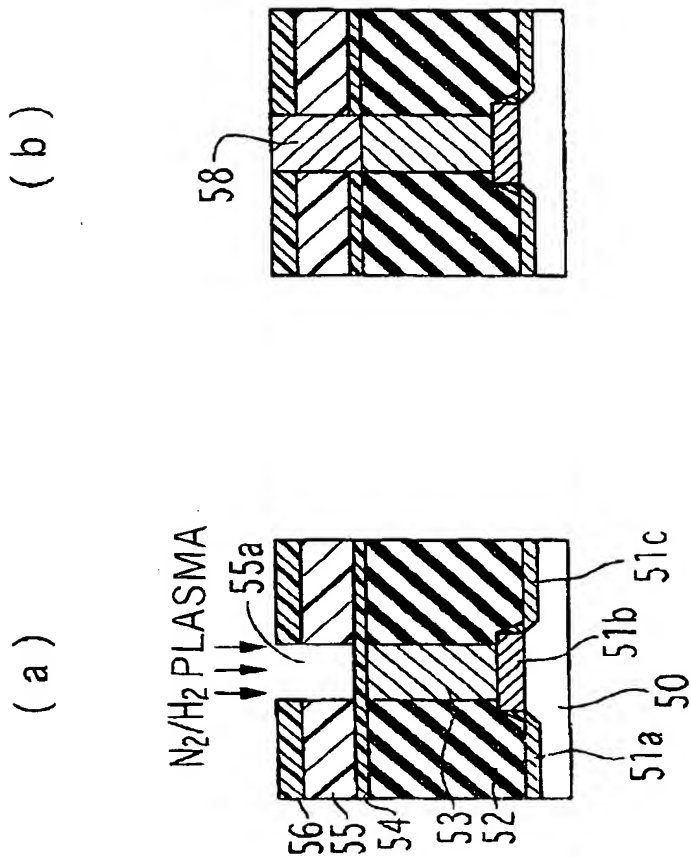


FIG.9

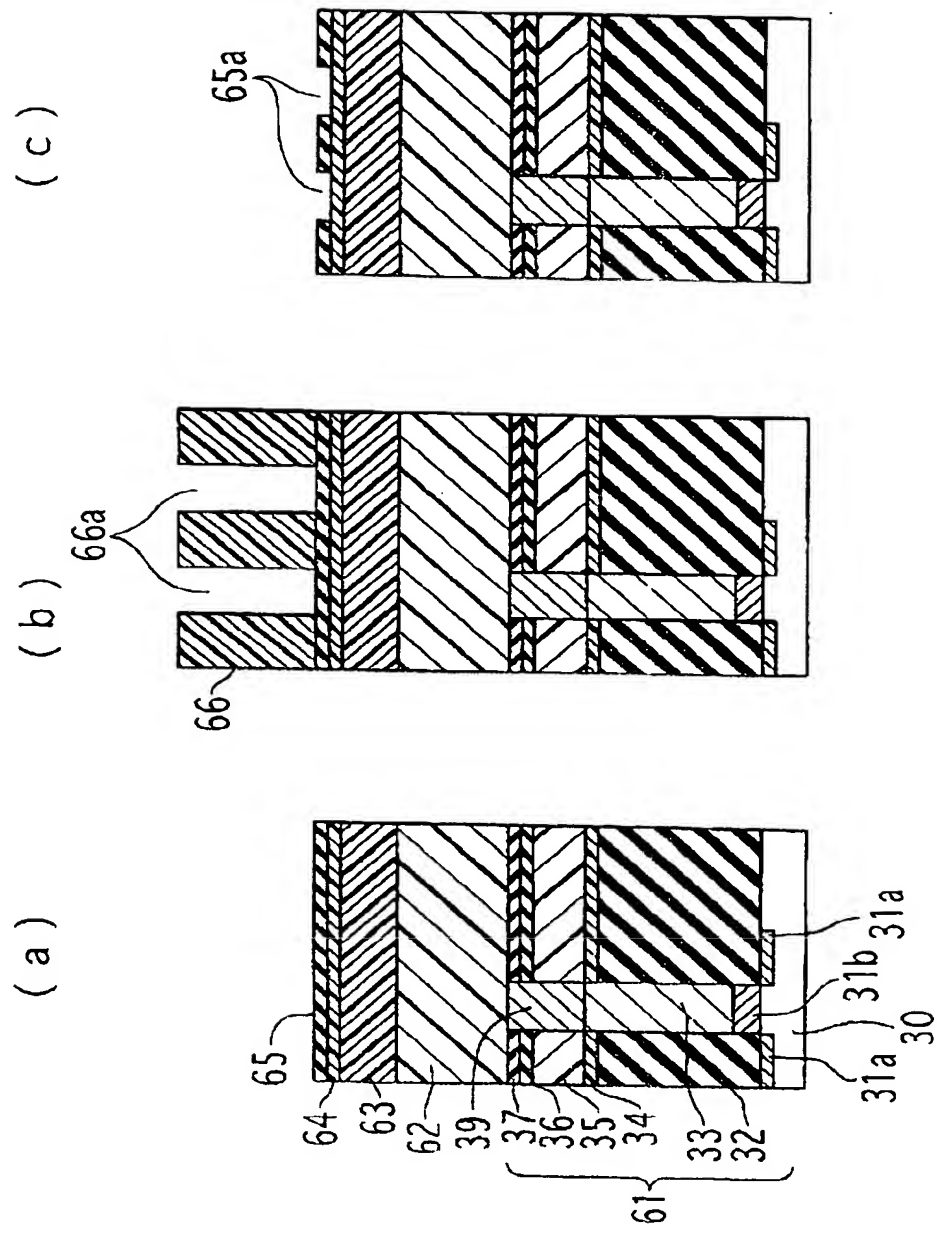


FIG.10

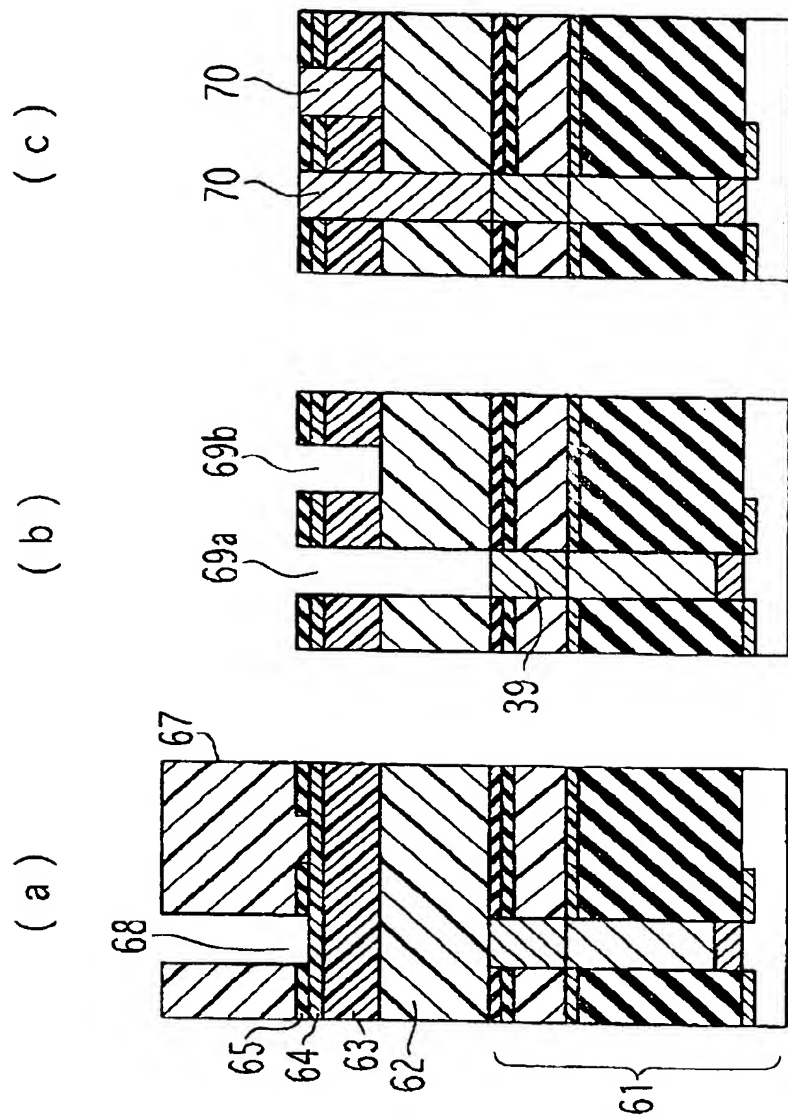


FIG. 11

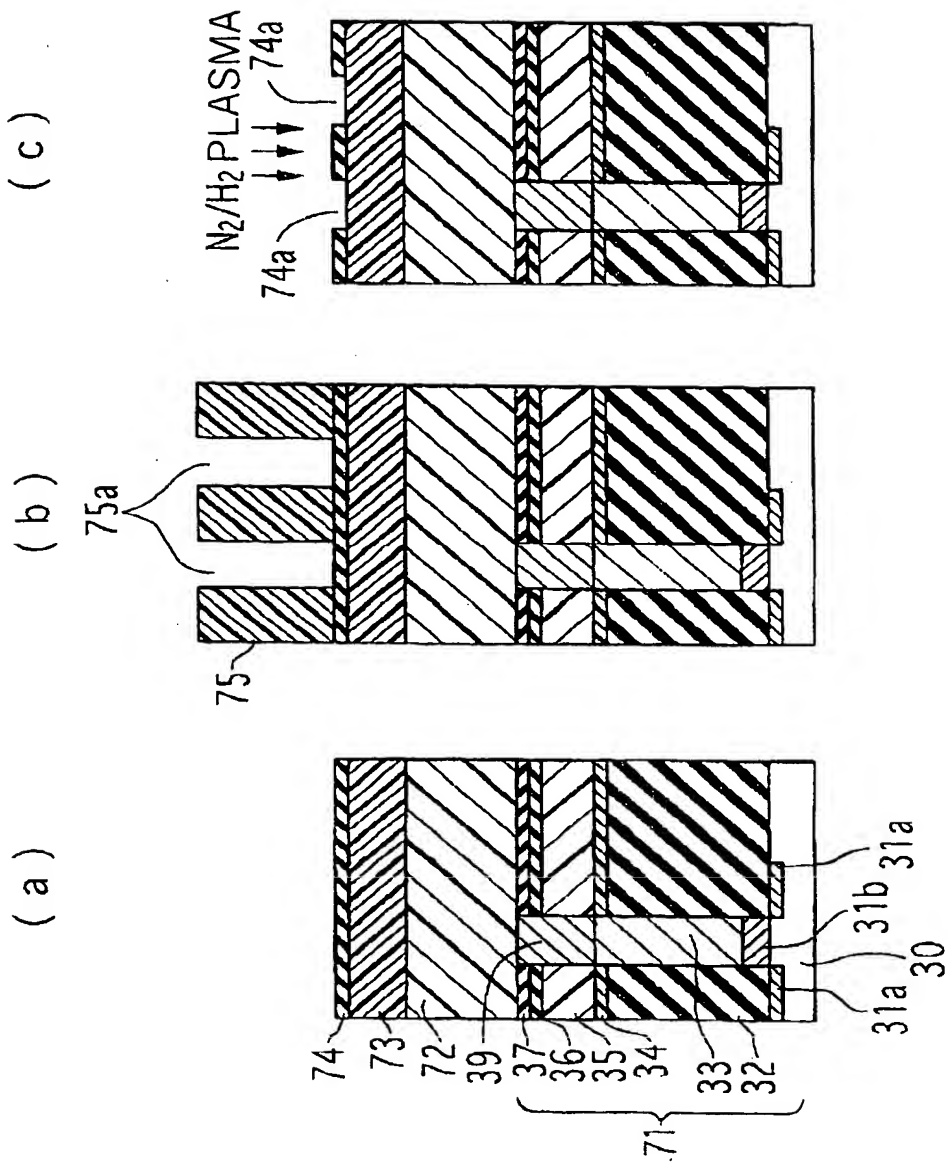


FIG.12

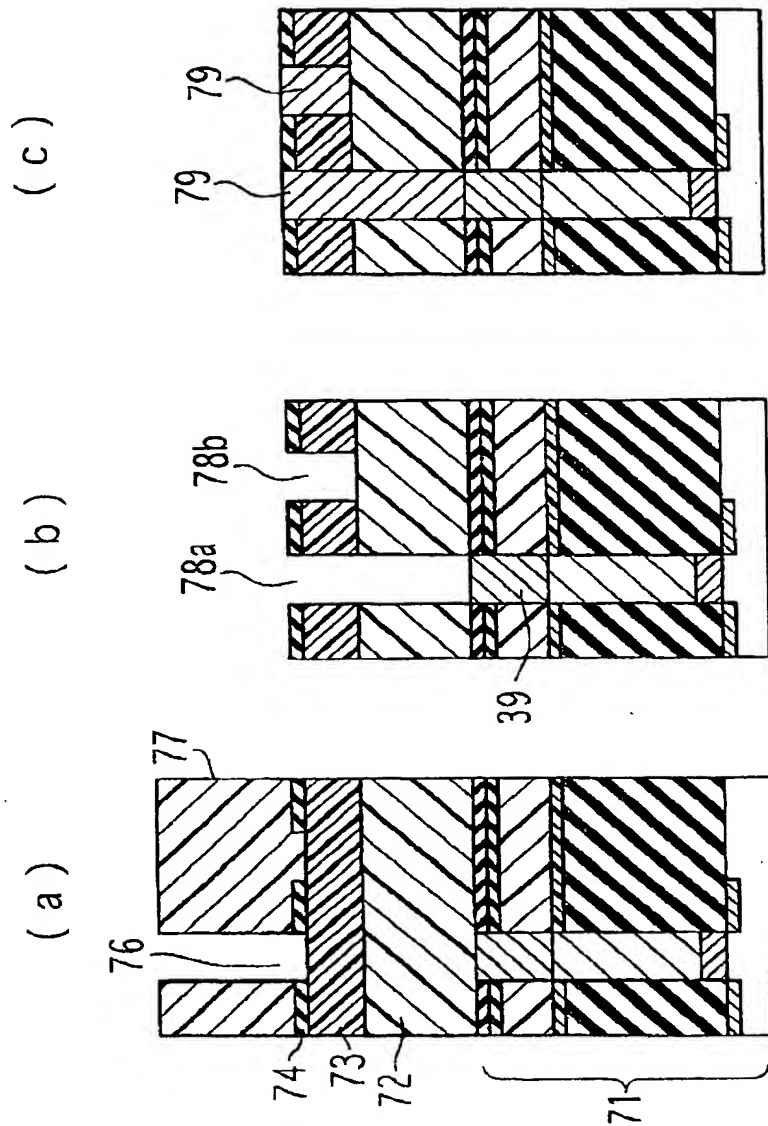


FIG. 13

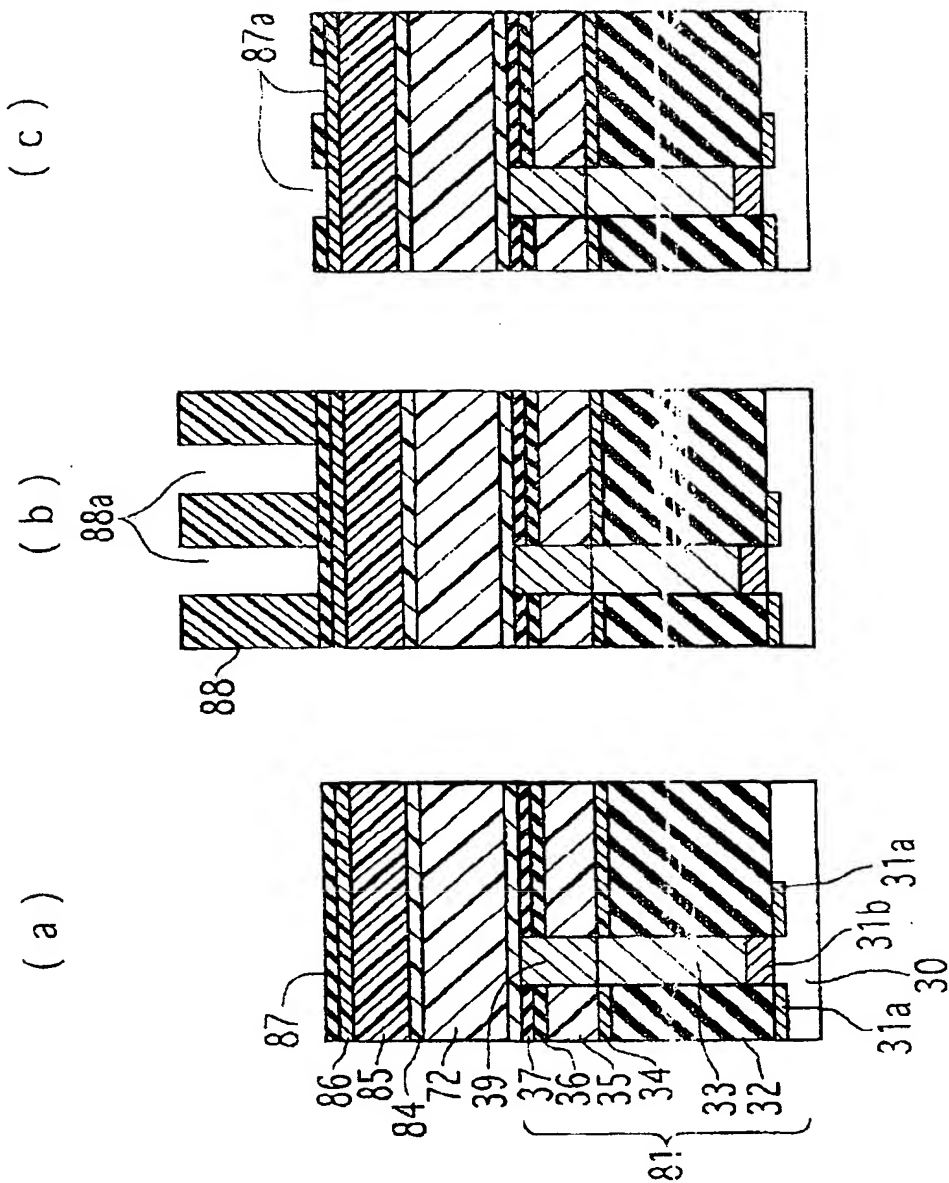


FIG.14

FIG. 15 is a cross-sectional view of a semiconductor device in a third state. The device includes a substrate 81, a gate stack 82, a gate electrode 83, a gate insulating layer 84, a gate conductive layer 85, a gate contact layer 86, a gate contact pad 87, a gate contact opening 88, and a gate contact plug 89. The gate contact plug 89 is formed in the gate contact opening 88 and is electrically connected to the gate contact layer 86. The gate contact pad 87 is formed on the gate contact layer 86 and is electrically connected to the gate contact plug 89. The gate conductive layer 85 is formed on the gate contact layer 86 and is electrically connected to the gate conductive layer 85. The gate insulating layer 84 is formed on the gate conductive layer 85 and is electrically connected to the gate insulating layer 84. The gate electrode 83 is formed on the gate insulating layer 84 and is electrically connected to the gate electrode 83. The gate stack 82 is formed on the gate electrode 83 and is electrically connected to the gate stack 82. The substrate 81 is formed on the gate stack 82 and is electrically connected to the substrate 81.

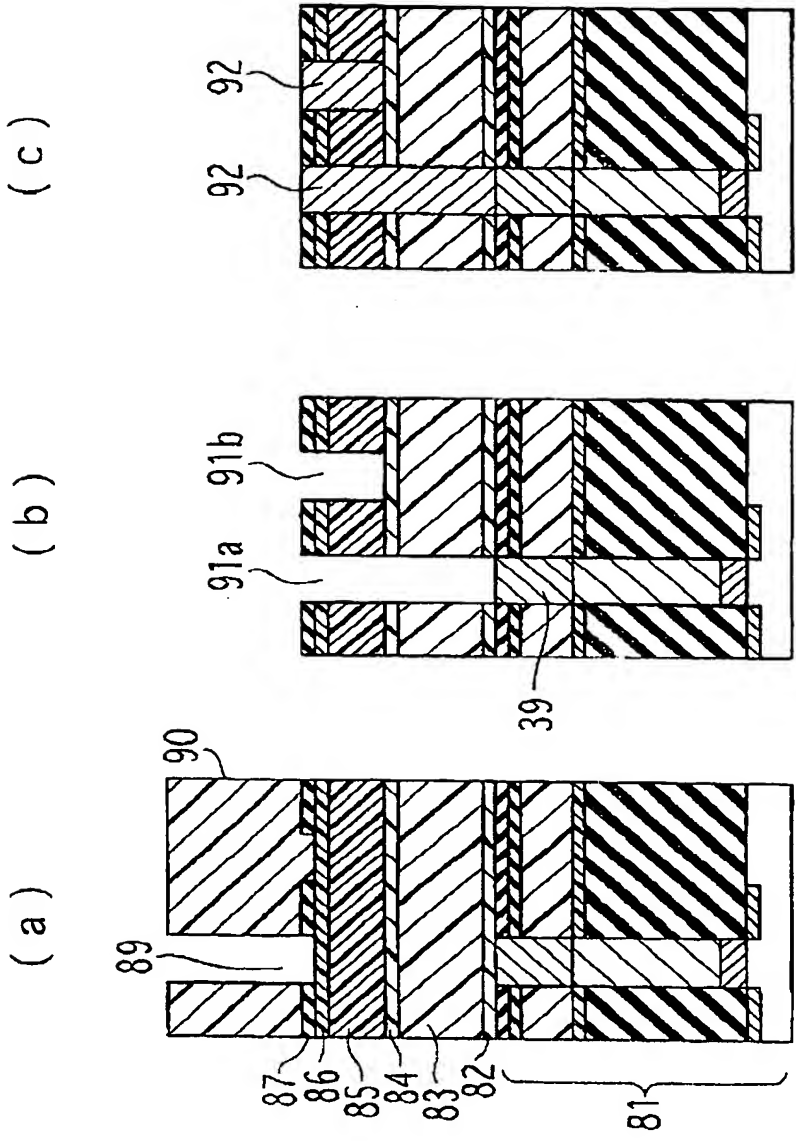


FIG.15

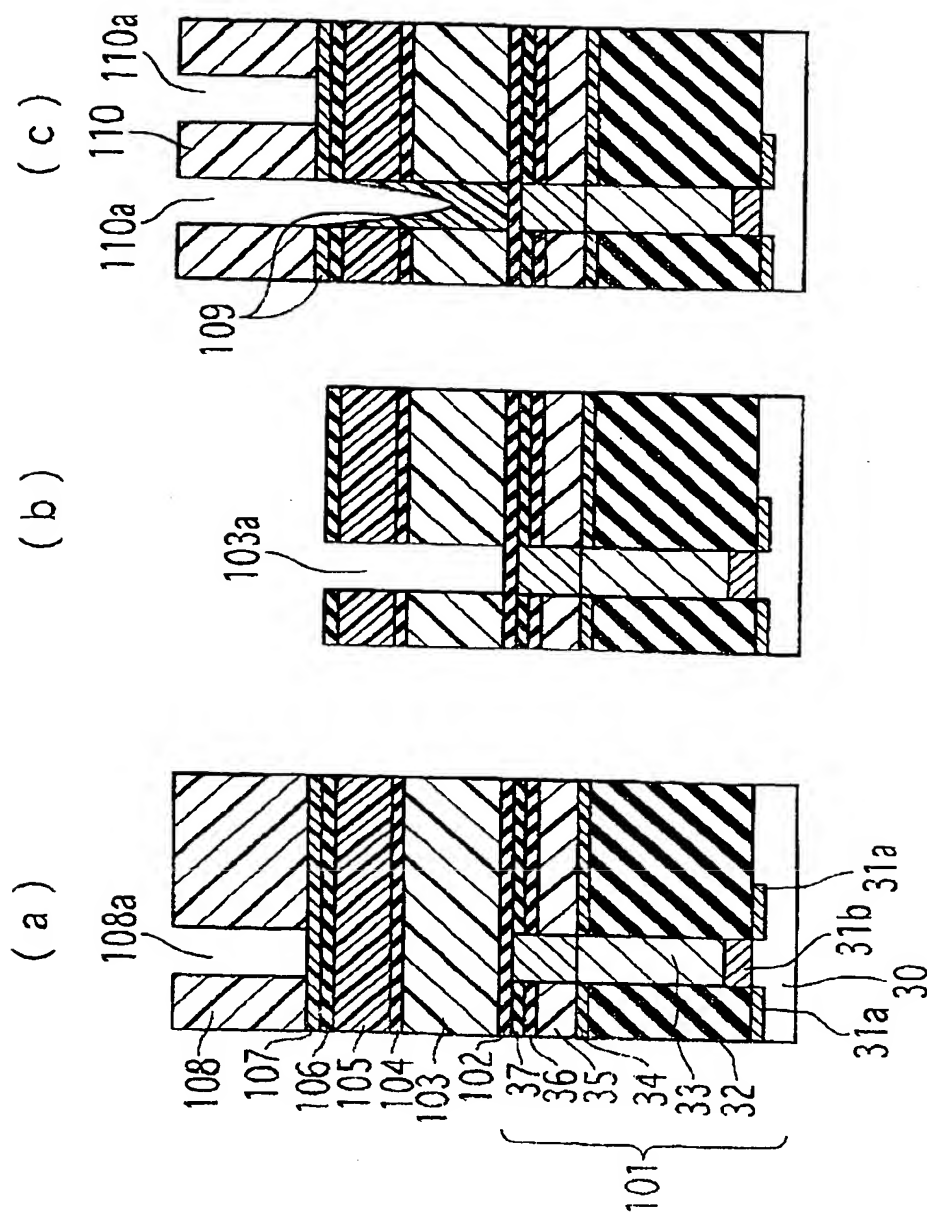


FIG.16

FIG. 17 is a cross-sectional view of a semiconductor device in a third stage of manufacturing, showing the formation of a second layer of material 105a on the first layer 105. The second layer 105a is formed by a process such as chemical vapor deposition (CVD) or atomic layer deposition (ALD). The second layer 105a is formed on the first layer 105 and the first layer 105 is formed on the substrate 101. The second layer 105a is formed on the first layer 105 and the first layer 105 is formed on the substrate 101.

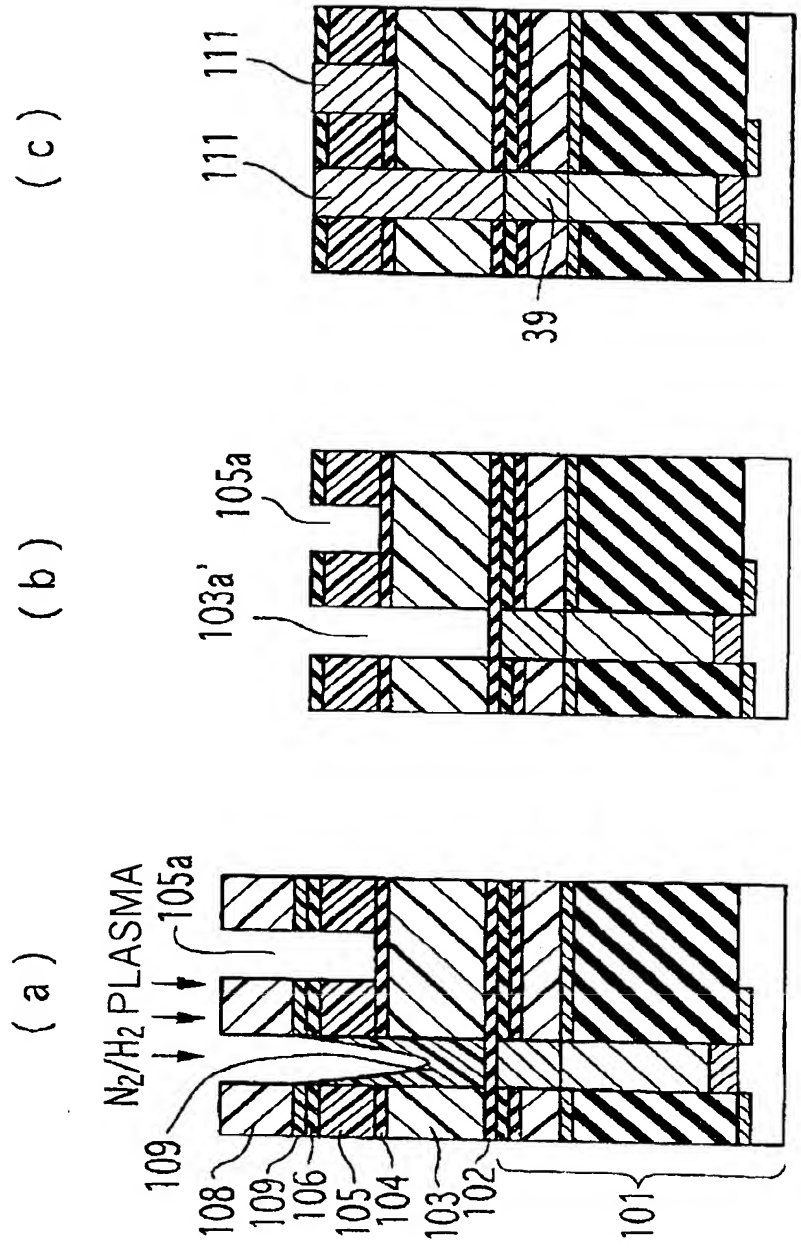


FIG.17

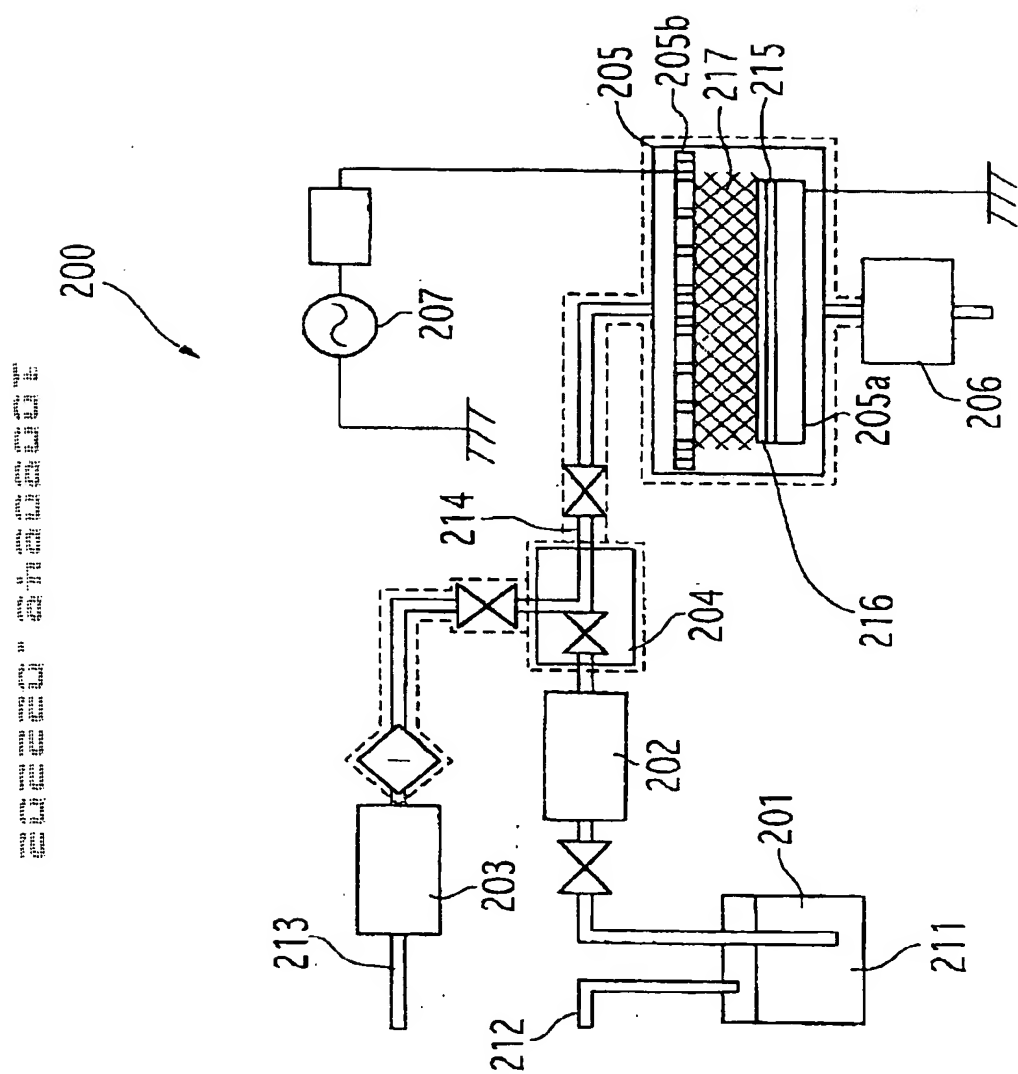


FIG. 18

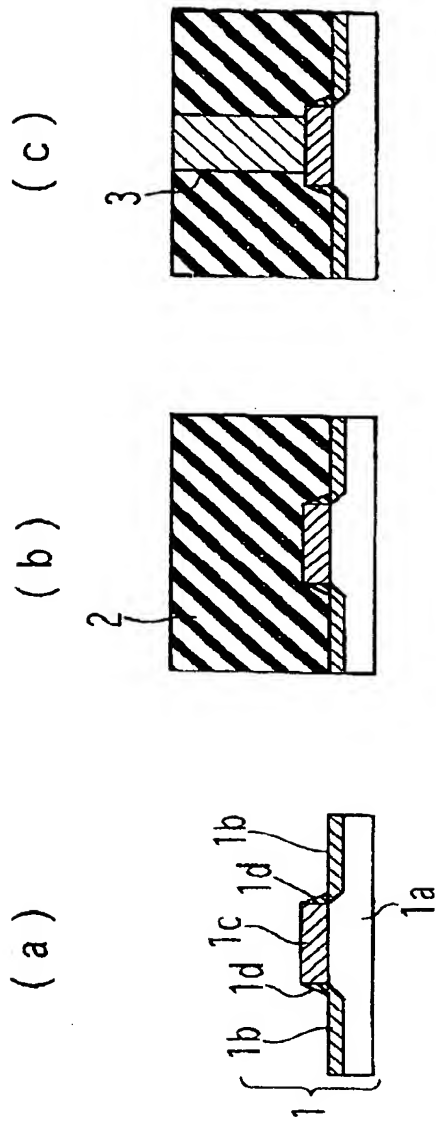


FIG.19

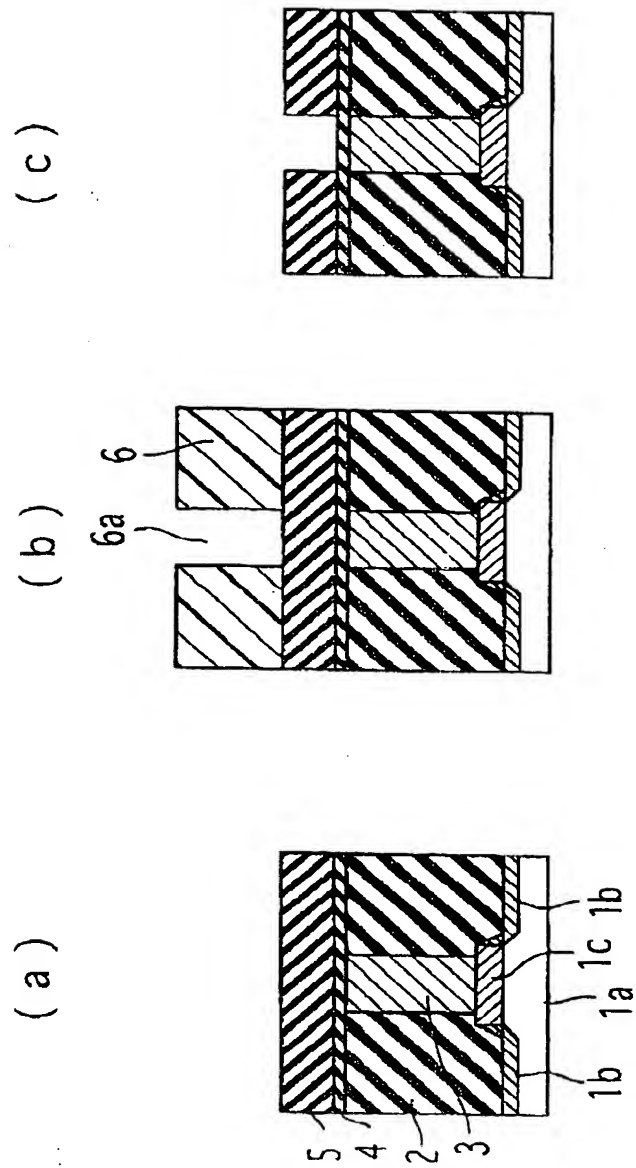


FIG.20

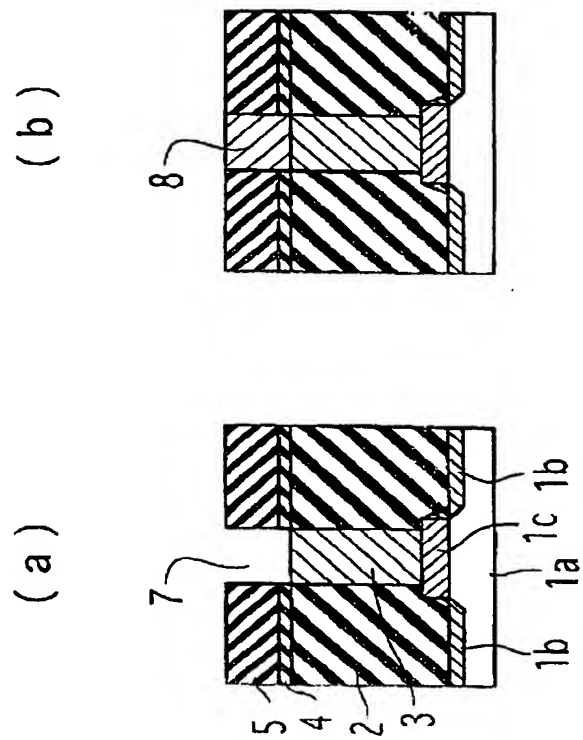


FIG.21

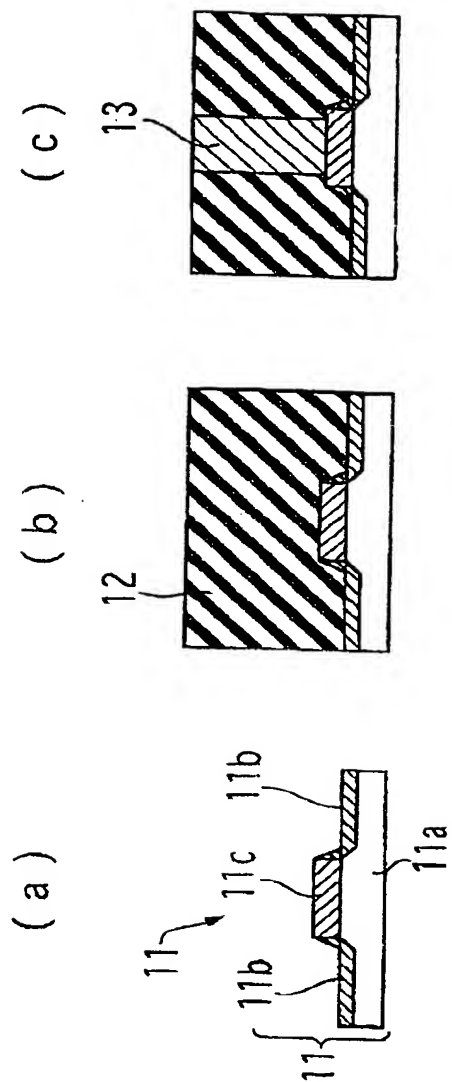


FIG.22

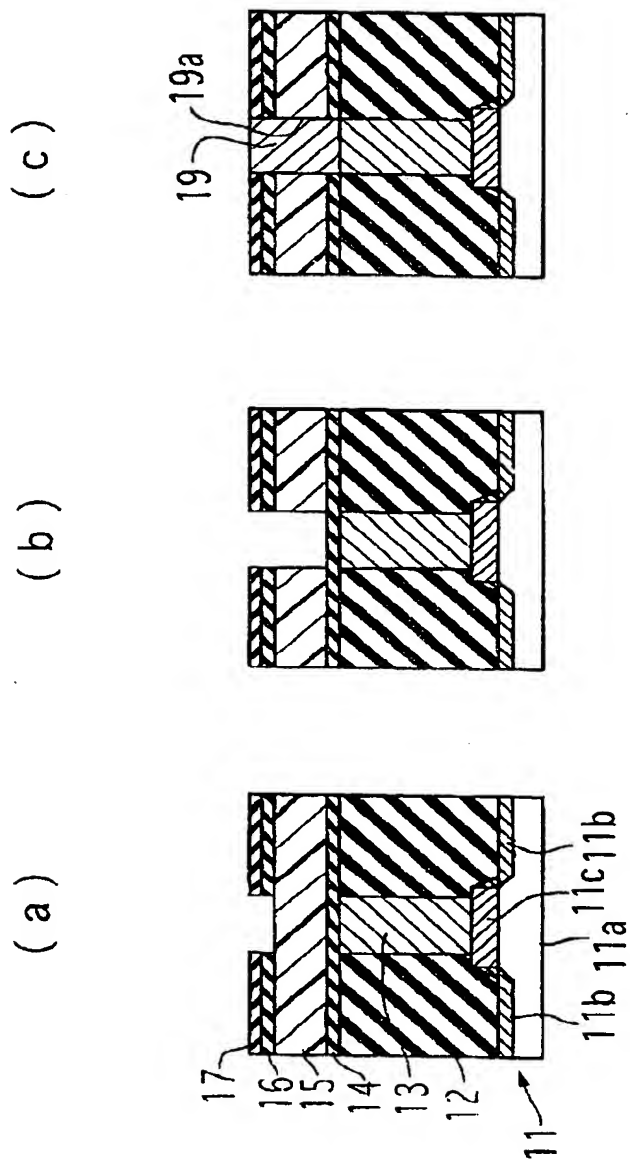
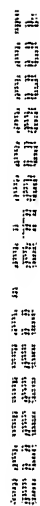


FIG.24

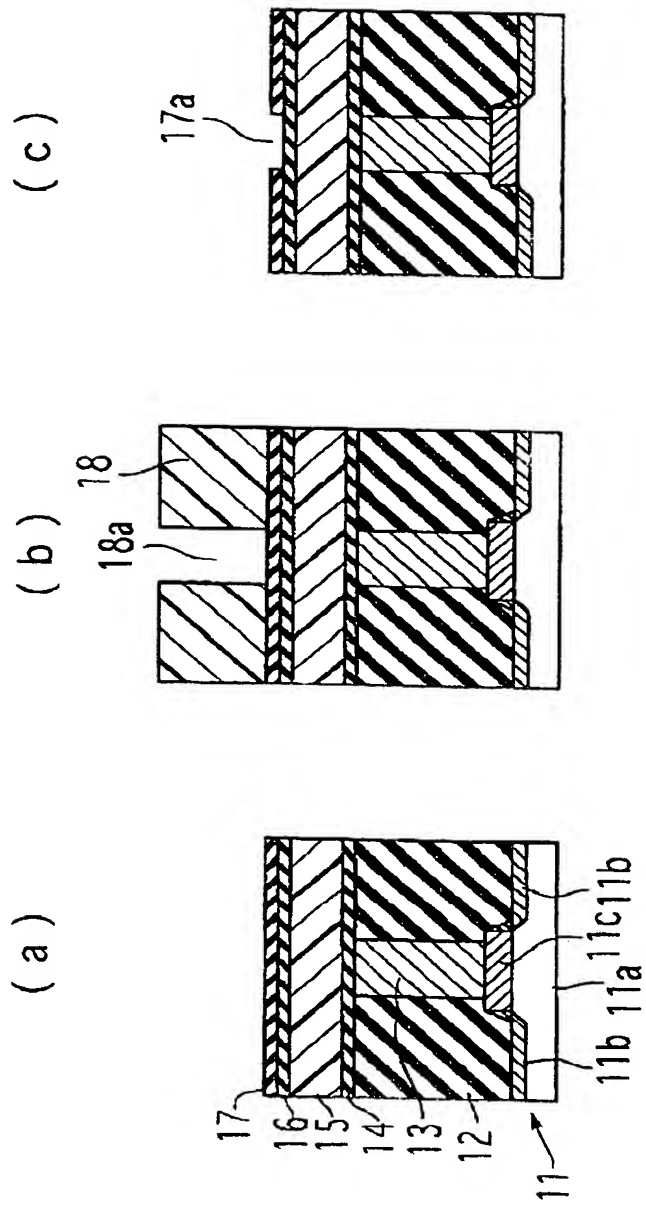


FIG. 23

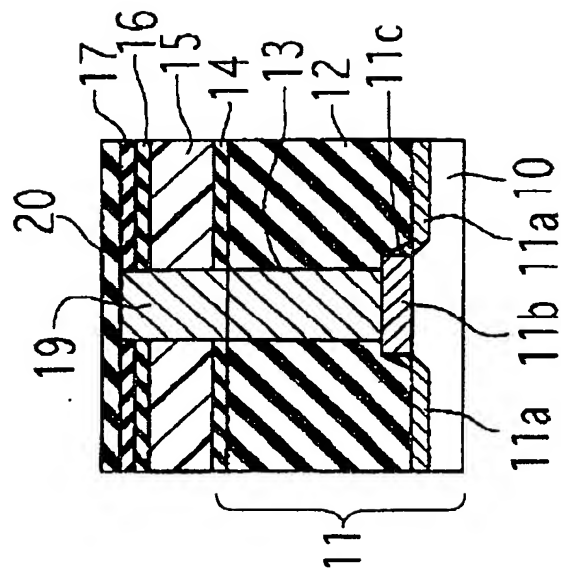


FIG. 25